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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,087	01/14/2004	Arup Bhattacharyya	MI22-2473	2443

21567 7590 08/22/2007

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
3663	

MAIL DATE	DELIVERY MODE
08/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/760,087	BHATTACHARYYA, ARUP	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *71-73,76,78-81,89 and 90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *71-73,76,78-81,89 and 90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/14/2007 has been entered.

Response to Amendment

Amendment filed 6/14/2007 with said Request for Continued Examination forms the basis for this Office Action. In said Applicant added new claims 89 and 90 and substantially amended all previously pending claims through substantial amendment of independent claim 71. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claim 71*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al (6,888750 B2) in view of Yamazaki et al (6,693,044 B1) and Yamazaki et al

(6,759,677 B1), henceforth referred to as "Yamazaki-1" and "Yamazaki-2", respectively.

Walker et al teach a computer system (col. 1) (e.g., logic circuits (Figures 12-14) together with the nonvolatile memory array (see "Field of Invention") constitute a computer system) with stacking according to the embodiment of Figure 9 (col. 14, l. 61-67)) comprising: a signal source capable to provide a data signal (from word line 445; col. 17, lines 60-65); and an inverter 443 coupled with the signal source (col. 17, l. 45-46), capable to invert the data signal and output the inverted signal (through bit lines 447); the inverter including (Figure 9, i.e., "CMOS array" "in pillar or self-aligned TFT configurations"):

a structure 413/415/417 comprising semiconductor material (Figure 11; see col. 15, l. 28 – 36) comprising at least silicon (col. 1,, l. 6-8);

a first transistor (PMOS TFT: see col. 14, l. 68 – col. 15, l. 2 on the inclusion of both options, PMOS with NMOS stacked thereon or *vice versa*) (with gate 243; Figure 9, and col. 11, l. 28-30) supported by the structure, the first transistor comprising a first gate 243 (Figure 9 and col. 11, l. 28-30) and first active region 219: Figure 9 and col. 11, l. 24-26) proximate the first gate; the first active region including a first channel region (219 = region between neighboring s/d regions 217) and a pair of first source/drain regions 217 (col. 11, l. 24-26); at least a portion of the first active region being within the structure (Figure 9), the first transistor being a PFET (i.e., a PMOS TFT: see col. 14, l. 68 – col. 15, 2 on the inclusion of both options, PMOS with NMOS stacked thereon or *vice versa*) and the first source/drain regions accordingly being p-doped regions; the

first gate being substantially non-overlapping with respect to the first source/drain regions (because the embodiment of Figure 9 has gates 243 and 217 in a substantially non-overlapping configuration as evident from Figure 9);

an insulative material 203 (col. 11, l. 42-44) over at least a portion of the first transistor (Fig.9);

a second transistor over the material layer and comprising a second gate 243 (col. 11, l. 2-8) and a pair of source and drain regions 217 (col. 11, l. 24-26), the second transistor being an NFET (NMOS TFT)) (Figure 9 and col. 14, l. 68 – col. 12, l. 2)) and the second source/drain regions accordingly being n-type doped regions (loc.cit.); the second gate being directly over the first gate (Figure 9: 243 being directly over each other); the second gate being substantially non-overlapping with respect to the second source/drain regions (because the embodiment of Figure 9 has gates 243 and 217 in a substantially non-overlapping configuration as evident from Figure 9);

the first and second gates being electrically connected to one another (see Figures 12-14 and col. 16, l. 58-60), and being in electrical connection with the signal source 471 (Figure 14); and

one of the first source/drain regions being electrically connected to one of the second source/drain regions and being in electrical connection with the output (Figure 14).

Although Walker et al do not specifically teach the structure of the specific embodiment of Figure 9 to comprising also germanium, it would have been obvious to comprise germanium in view of the teaching by Walker et al in a non-volatile memory

array (Figure 1 and cols. 2-3), hence analogous art, that germanium addition may be advantageously used as a seed for the crystallization of amorphous silicon (comprising silicon and germanium (see col. 3, l. 28-41)). *Motivation* for inclusion of the teaching by Walker et al also for the CMOS TFT array as described above derives from the resulting advantage of thus achieving polysilicon mobility through efficient manufacturing from a relatively cheap source material (amorphous silicon).

Walker et al do not necessarily teach the limitation "a first layer of semiconductive material over the insulative material; a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material", i.e., lines 13-17 of claim 71.

However, it would have been obvious to include said further limitation in view of Yamazaki-1, who, in a patent on TFTs (thin film transistors) (cols. 1-2), hence analogous art (see Walker et al, cols. 12-14), teach in their Embodiment 2 (cols. 8-10) the TFT to be supported by a first layer of semiconductive material 202 (see Figures 2, col. 8, l. 39-49 and col. 9, l. 1-30) over insulative material 200 (loc.cit.) and a second layer of semiconductive material 204 (col. 9, l. 35-67) physically contacting the first layer of semiconductive material (see Figure 2E and col. 9, l. 35-39), and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material (nickel does exist in 202, and the concentration of nickel, in expression of contrast according to Yamazaki-1, exists hardly in 204: see col. 10, l. 1-5).

Motivation to include the teaching by Yamazaki-1 in the invention by Walker et al derives from the improved device characteristics by virtue of the strongly reduced nickel content of the second semiconductive material layer, which supports the active region of the TFT (col. 10, l. 1-19, especially l. 1-5).

Although Yamazaki-1 appears to specifically only teach the application of his teaching to silicon semiconductive material for the channel supporting layers, Yamazaki_2 actually teach the application of nickel as a catalyst for crystallization through anneal and the use of laser annealing not only for silicon but equally for silicon-germanium (see "Background of the Invention" for the teaching of the reason why application is extended to silicon-germanium, i.e.,.increased mobility: col. 1, l. 5-65; and see col. 4, l. 24-28), and hence provides testimony of both the *combinability* and the motivation to include application also to silicon-germanium as the basic material for the semiconductor films.

N.B.: Drawings and pictures can anticipate claims if they clearly show the structure which is claimed. *In re Mraz, 455 F.2d 1069, 173 USPQ 25 (CCPA 1972).*

1. ***Claims 72-73, 76, 80-81, 89 and 90*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al, Yamazaki_1 and Yamazaki_2 as applied to claim 71 above, and further in view of Bulsara et al (US 2003/0030091 A1).

As detailed above, claim 71 is unpatentable over Walker et al in view of Yamazaki-1 and Yamazaki-2. None necessarily teach the further limitations defined by claims 72, 73, 80 or 81.

However, it would have been obvious to include said limitations in view of the teaching as prior art by Bulsara et al that relaxed silicon-germanium including a strained layer 18 formed of silicon ([0036], hence claim 73 is also met and, being a SiGe layer ([0036], claim 76 is also met) (i.e., layer with strained lattice, hence inherently crystalline in addition to being strained) and a relaxed underlying silicon-germanium (hence claim 80 also met) crystalline layer 14 ([0035]) (with from 20 to 90 % germanium, hence claim 81 is met because there necessarily is one % value contained in the claimed range) directly applied on a graded silicon-germanium (SiGe) layer 12 (loc.cit.) (i.e., on top of a crystalline silicon-containing layer (inherently crystalline, because without being crystalline here cannot be a grading of the lattice constant (see [0003]) so as to produce field effect transistors (FETs) with increased channel mobility, hence improved device speed (loc.cit.) Implementation of the teaching for both the NFET and the PFET by Walker et al necessarily leads to the claimed device because the source/drain regions in Walker et al extend throughout the entire silicon substrate, being members of a poly bit line 333 (see Figure 10A, and see column 13, lines 20-28).

Motivation to include the teaching by Bulsara et al in the invention by Walker et al derives at least from the resulting improvement in device speed as taught by Bulsara (loc.cit.).

On claim 89: in Walker et al (Figure 9) the first channel region 219 is between the source/drain regions 217; the first gate 243 is above the first channel region; and the width of the first gate with respect to a cross sectional view of the inverter is substantially the same as the width of the first channel region 219 with respect to the

cross sectional view (said cross-sectional view being defined by the source-drain connection and normal to the upper main surface of source/drain regions). See Figure 9.

On claim 90: in Walker (Figure 9) the first gate 243 is neither above nor below the first source/drain regions 217 and the second gate 243 is neither above nor below the second source/drain regions 217 (Figure 9).

2. ***Claims 78 and 79*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Walker et al, Yamazaki-1, Yamazaki-2 and Bulsara et al as applied to claim 72 above, and further in view of Hsu et al (6,793,731 B1).

As detailed above, claim 72 is unpatentable over Walker et al in view of Yamazaki-1, Yamazaki-2 and Bulsara et al, none necessarily teaching the further limitation defined by claim 78 or claim 79. However, said limitations would have been obvious over Hsu et al, who teach as prior art polycrystalline SiGe (cols. 1-2), while teaching as improvement thereof single-crystal relaxed SiGe free of defects (abstract and col. 2, l. 65 – col. 5, l. 65). It has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

Response to Arguments

Applicant's arguments filed 6/14/07 have been fully considered but they are not in every respect persuasive. Specifically, although examiner agrees with applicant's first argument (page 8+ of Remarks) on the different nature of the devices of Figures 10A

and 13, a rejection based on the same prior art can be provided based on the CMOS pillar or self-aligned TFT configuration of Figure 9 as the arrangement of the CMOS array in the logic circuits of Figures 12-14, as shown by the rejections overleaf, which are herewith included by reference in their entirety in response to applicant's traverse.

In response to applicant's second argument of traverse (page 10 of Remarks) on limitations not disclosed by Walker et al, examiner respectfully points out that neither the previous rejections nor the rejections overleaf rely on any teaching by Walker et al on "a second layer of semiconductive material physically contacting a first layer of conductive material" as claimed, but instead relied, respectively rely on obviousness over Yamazaki-1 in this regard; while the first and second gate being substantially non-overlapping with respect to the first and second source/drain regions, respectively, is clearly (Figure 9) met by the embodiment of the CMOS pillar or self-aligned TFT configuration of Figure 9, in which gates 243 and source/drain regions 217 are substantially non-overlapping as shown in three dimensional representation.

In light of the above, and after examination of new claims 89 and 90, all claims are rejected over the prior art as cited.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
August 18, 2007

Primary Patent Examiner:
Johannes Mondt (TC 3600, Art Unit: 3663)